DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4-5, 7-8, 10-11, 13-23, and 32-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al (2003/0025459) hereinafter, Lee.

3. In regards to claim 1, Lee teaches a plasma display, comprising (abstract):

a panel forming an equivalent panel capacitor (fig. 2 and 13 Cp);

a first voltage source to charge the panel to a first polarity, voltage (fig. 2 and 13 Vs); and

a second voltage source to charge the panel to a second polarity voltage different from the first polarity voltage (fig. 2 and 13 (-Vs))

an inductor for recovering an energy stored in the panel by a resonance phenomenon (abstract) such that the recovered energy is reusable for driving the panel (fig. 2 and 13 (L));

first (fig. 13 S3) and second (fig. 13 S4) switches arranged, in parallel, between the inductor and the panel capacitor (fig. 2 and 13 (S3 and S4)),

a third switch arranged between the first voltage source and the panel (fig. 13 (S2): and

a fourth switch arranged between the second voltage source and the panel (fig. 13 (S1)), wherein the inductor stores energy recovered from the panel when the first switch is on ([0050] M1 S3) and the inductor applies the stored energy to the panel when the second switch is on ([0052] M3 S4), and wherein the inductor stores the energy at a time when a sustain voltage supplied to the panel is clamped at a predetermined voltage (Vy is clamped at Vs and is in M1 wherein the inductor stores energy), and during at least a period of driving the plasma display, the first switch and the fourth switch are turned on together or the second switch and the third switch are turned on together (fig. 3 S1 and S3:On) .

4. In regards to claim 5, Lee teaches an energy recovering method for a plasma display, comprising (abstract):

forming a first electrically conductive path between a first voltage source and the plasma display using a first switch (fig. 3 M1 and S1);

forming a second electrically conductive path between a second voltage source and the plasma display using a second switch (fig. 3 M3 S2) ;

forming a third electrically conductive path between an inductor and the plasma display using a third switch (fig. 3 (M2) S3); and

forming a fourth electrically conductive path between the inductor and the plasma display using a fourth switch connected, in parallel, to the third switch (fig. 3 (M4) S4),

said method further comprising:

shutting off a backward current from the plasma display using a first diode connected between the third switch and the plasma display (fig. 13 (D1)); and

shutting off a backward current from the fourth switch using a second diode connected between the fourth switch and the plasma display (fig. 13 (D2)),

wherein the inductor stores energy recovered from the plasma display wherein a sustain voltage applied to the plasma display is clamped at a predetermined voltage when the second switch is closed (fig. 3 Vy clamped at Vs at M2 S2 off), and current of the inductor is increased or decreased prior to discharging of a display capacitance ([0050-00053)] fig. 3 (half period of sine wave).

5. In regards to claim 7, Lee teaches a plasma display comprising (abstract):

a display having a plurality of electrodes and having a corresponding panel capacitance between first and second nodes (fig. 13 (Cp Vy is first node and second node is other side of Cp));

an inductor (fig. 13 (L)) coupled to the second node (fig. 13 coupled to Vy through various other paths, i.e. through S3 or through ground) and a third node (fig. 13 node connected to S3 and S4); a first switch coupled between the first and third nodes (fig. 13 S3); and a second switch coupled between the first and third nodes (fig. 13 S4), the first and second switches being formed in parallel [0046], wherein a first current path is formed via the panel capacitance [0050-0053], the second node, the inductor, the third node, the first switch and the first node (fig. 3 M1 and fig. 13 S3 ON), and a second

current path is formed via the panel capacitance, the first node, the second switch, the third node, the inductor and the second node (fig. 3 M3 [0050]), and

wherein the second current path passes energy from the panel capacitance for storage in the inductor when the second switch is on [0050], and the first current path applies the stored energy from the inductor to the panel capacitance when the first switch is on [0053], and wherein the inductor stores energy recovered from the panel capacitance and a sustain voltage applied to the panel capacitance is clamped at a predetermined voltage when the second switch (fig. 3 Vy clamped at Vs) is on and current of the inductor is increased or decreased [0025] prior to discharging of the panel capacitance (fig. 9 [0069-0080]). Examiner notes as shown in fig. 9, S2 and S3 are on at the same time. And thus, IL will accumulate charge before S2 is turned off and it is applied to Cp.

6. In regards to claim 19, Lee teaches in display panels having panel electrodes and corresponding panel capacitance (fig. 13 Cp) between first (fig. 13 node at Vy) and second nodes (fig. 13 Cp node at sustain-discharge circuit), an inductor coupled to the second node (fig. 13 coupled to Vy through various other paths, i.e. through S3 or through ground) and a third node (fig. 13 node connected to S3 and S4); a first switch coupled between the first and third nodes (fig. 13 S3) and a second switch coupled between the first and third nodes (fig. 13 S4), the first and second switches being formed in parallel [0046], an energy efficient method of driving said display panels

through the inductor coupled to the panel electrodes, comprising (abstract and [0046-0053]):

(a) discharging the panel capacitance through said inductor initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum through a first current path formed via the panel capacitance [0046-0050], the second node, the inductor, the third node, the first switch and the first node, and secondly charging the panel capacitance through said inductor while removing the stored energy from said inductor until the inductor current reaches zero or before zero via the first current path (fig. 3 IL [0050]) ; and

(b) discharging the panel capacitance through said inductor initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum through a second current path formed via the panel capacitance, the first node, the second switch, the third node, the inductor and the second node, and secondly charging the panel capacitance through said inductor while removing the stored energy from said inductor until the inductor current reaches zero or before zero through the second current path [0053] and [0055],

wherein said inductor stores said energy while the panel capacitance is clamped at first predetermined voltage and wherein said energy is removed from said inductor to cause the panel capacitance to change to a second predetermined voltage [0046-0049] and

wherein current of the inductor is increased during a previous period of discharging the panel capacitance of (a), and current of the inductor is decreased during

a previous period of discharging the panel capacitance of (b) (fig. 9 IL starts to increase before Vs)

7. In regards to claim 4, Lee teaches the plasma display as claimed in claim 1, further comprising: a first diode connected between the first switch and the panel (fig. 13 d1); and a second diode connected between the second switch and the panel (fig. 13 d2).

8. In regards to claim 8, Lee teaches the plasma display of claim 7, wherein the direction of the first and second current paths are opposite directions (fig. 3 M1 and M3). Examiner notes the current paths are in opposite direction since one charges voltage in the panel capacitor and the other direction stores current in the inductor.

9. In regards to claim 10, Lee teaches the plasma display of claim 7, wherein the panel display capacitance is charge or discharged based on an LC resonance frequency [0046 and 0050].

10. In regards to claim 11, Lee teaches the plasma display of claim 10, wherein the panel display capacitance is charged or discharged based on a non-LC resonance frequency.[0050 and 0055].

11. In regards to claim 13, Lee teaches the plasma display of claim 11, wherein during charging or discharging, the panel capacitance is clamped before a stored energy of the inductor reaches zero (fig. 9 Vs clamped and IL).

12. In regards to claim 14, Lee teaches the plasma display of claim 7, wherein the first current path further comprises a diode coupled between the first switch and the first node (fig. 13 D1 in-between Vy).

13. In regards to claim 15, Lee teaches the plasma display of claim 7, wherein the second current path further comprises a diode coupled between the first node and the second switch (fig. 13 D2 in-between Vy).

14. In regards to claim 16, Lee teaches (Original) The plasma display of claim 7, further comprising: a first clamping circuit coupled between the first and second nodes ; and a second clamping circuit coupled between the first and second nodes (fig. 13 S1 and S2 is “coupled” between the first and second nodes).

15. In regards to claim 17, Lee teaches the plasma display of claim 16, wherein the first clamping circuit comprises a third switch coupled to the first node and a first potential via a first conductive path, and the second clamping circuit comprises a fourth switch coupled to the first node and a second potential via a second conductive path, wherein the first and second potentials are different (fig. 13 S1 and S2 is “coupled” between the first and second nodes [0046-0055]).

16. In regards to claim 18, Lee teaches the plasma display of claim 17, wherein the first potential is provided by a positive power source, and the second potential is provided by a negative power source (fig. 13 Vs and –Vs).

17. In regards to claim 20, Lee teaches the method of claim 19 further comprising: maintaining panel capacitance after step (a) by a first clamping circuit having a third switch coupled to the first node and a first potential via a first conductive path; and

maintaining the panel capacitance (fig. 13 S1) after step (b) by a second clamping circuit having a fourth switch coupled to the first node and a second potential via a second conductive path (fig. 13 S2) [0046-005].

18. In regards to claim 21, Lee teaches the method of claim 20, wherein storing and removing of stored energy in the inductor is based on an LC resonance frequency if the inductor current reaches zero [0046-0050] and fig. 9 IL).

19. In regards to claim 22, Lee teaches the method of claim 20, wherein charging and discharging of the panel capacitance is not based on an LC resonance frequency via the first and second clamping circuit clamping the panel capacitance prior to the inductor current reaching zero [0046-0050, 0069-0072] and fig. 9 IL).

20. In regards to claim 23, Lee teaches the method of claim 22, wherein the first and second clamping circuits clamp the panel capacitance prior to the inductor current reaches zero [0055, 0069-0072] and fig. 9 IL).

21. In regards to claim 32, Lee teaches the plasma display as claimed in claim 1, wherein the inductor stores the energy during a time when the sustain voltage supplied to the panel is clamped at a negative voltage (fig. 9 –Vs and IL Lee).

22. In regards to claim 33, Lee teaches the plasma display as claimed in claim 32, wherein the second switch is turned on to allow the inductor to apply the stored energy to the panel when the sustain voltage is to rise to a positive voltage (figs. 9 and 13, S4 M6 [0075].

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

25. Claims 25-29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (2003/0025459) hereinafter, Lee in view of Rilly et al (5,808,420), hereinafter, Rilly.

26. In regards to claim 25, Lee teaches a plasma display panel driver circuit comprising (abstract):

a panel inter-electrode capacitor provided between at least one of a plurality of scanning electrodes and a plurality of sustain electrodes of a panel (fig. 13 Cp);

a charging/discharging circuit directly connected in series with said panel inter-electrode capacitor and between first and second nodes (fig. 13 S3 and S4),

a clamping circuit having first and second switches for clamping a terminal voltage across the panel inter-electrode capacitor to a first power source voltage level and to a second power source voltage level, said first switch being connected in series between the first node (fig. 13 S1, S2, Vs, and -Vs) and

the first power source voltage level (fig. 13 Vs), said second switch being connected in series between said first node and the second power source voltage level (fig. 13 Vy first node, and in series with –Vs), said inter-electrode capacitor being connected in series to the first and second nodes and said charging/discharging circuit and said clamping circuit being coupled in parallel between the first and second nodes (fig. 13 Cp in series with Vy and node at (S3 and L)),

wherein said charging/discharging circuit comprises a pair of switches coupled in parallel to each other between the first node and a third node and an inductive coil coupled in series between the second and third nodes (fig. 13 Vy and node between L and S3/S4),

wherein the inductive coil stores energy recovered from the panel inter-electrode capacitor when a first one of the pair of switches is turned on and the inductive coil applies the stored energy to the panel inter-electrode capacitor when a second one of the pair of switches is turned on [0050-0055], and wherein the clamping circuit increases or decreases energy of the inductor coil prior to discharging of the inter-electrode capacitor.

Lee fails to teach wherein the inductive coil is coupled to the first power source voltage level and the second power source voltage level along signal paths that do not pass through any of the first or second switches or the pair of switches.

However, Rilly teaches wherein the inductive coil is coupled to the first power source voltage level and the second power source voltage level along signal paths that do not pass through any of the first or second switches or the pair of switches.

It would have been obvious to one of ordinary skill in the art to have modified the power source and inductor connections of Lee to provide wherein the inductive coil is coupled to the first power source voltage level and the second power source voltage level along signal paths that do not pass through any of the first or second switches or the pair of switches as taught by Rilly in order to facilitate another path for chagrining and discharging the inductor, while also provides a means to ground a circuit, and provide a common return path for electric current.

27. In regards to claim 26, Lee as modified by Rilly teaches the plasma display panel driver circuit of claim 25, wherein each of the pair of switches comprises a first transistor and a diode, and the pair of switches provide opposite current paths (fig. 13 SS3, D1, S2 and D2 [0050-0055] Lee).

28. In regards to claim 27, Lee as modified by Rilly teaches the plasma display panel driver circuit of claim 25, wherein the inter- electrode capacitor is charged/discharged based on an LC resonant frequency of the inductor coil and the inter-electrode capacitor ([0046-0055] Lee).

29. In regards to claim 28, Lee as modified by Rilly teaches the plasma display panel driver circuit of claim 25, wherein the inter- electrode capacitor is charge/discharged based on a non-LC resonant frequency of the inductor coil and the inter-electrode capacitor ([0046-0055] Lee).

30. In regards to claim 29, Lee as modified by Rilly teaches wherein the clamping circuit clamps the inter-electrode capacitor one of the first and second power source voltage level prior to an energy of the inductor coil reaching zero (fig. 9 IL [0069-0071] Lee).

31. In regards to claim 31, Lee as modified by Rilly teaches the plasma display panel driver circuit of claim 25, wherein each of said first and second switches comprises a transistor (fig. 13 S3 and S4 MOSFET transistors [0047] Lee).

Response to Arguments

32. Applicant's arguments with respect to claims 1, 4-5, 7-8, 10-11, 13-23, 25-29, and 31-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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